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(54) Abstract Title
Video signal processor for received interlaced format video signals from different sources

(57) A video signal processor prevents image disturbances when switching between a first interlaced scanning format input signal eg a 30Hz NTSC signal, and a second similarly interlaced input signal but which has been converted from a progressively scanned format signal eg a 24Hz frame scanning frequency telecine film signal. When the first signal is input a mode discriminating signal from discriminator 117 switches selectors 107-110 to their L terminals so that mixer/selector 111 receives a motion signal from motion detector 106 and in response thereto adaptively mixes the outputs of inter-field interpolation field delay circuit 102 and intra-field line-interpolation filter 103. When the second signal is input selectors 107-110 are switched to their H terminals and mixer/selector 111 selects either this second input signal from selector 108 or the output of field delay circuit 105 according to film field indexes in the input signal detected by discriminator 117. When the input signal is changed-over from the first to the second signal, mixer/selector 111 receives the motion signal from discriminator 117 and selects the output from interpolation filter 103 for at least one field of the changed-over signal. The outputs from selector 107 and mixer/selector 111 are time compressed 112,113 and alternately selected at line frequency to provide a progressively scanned format signal eg for LCD display.

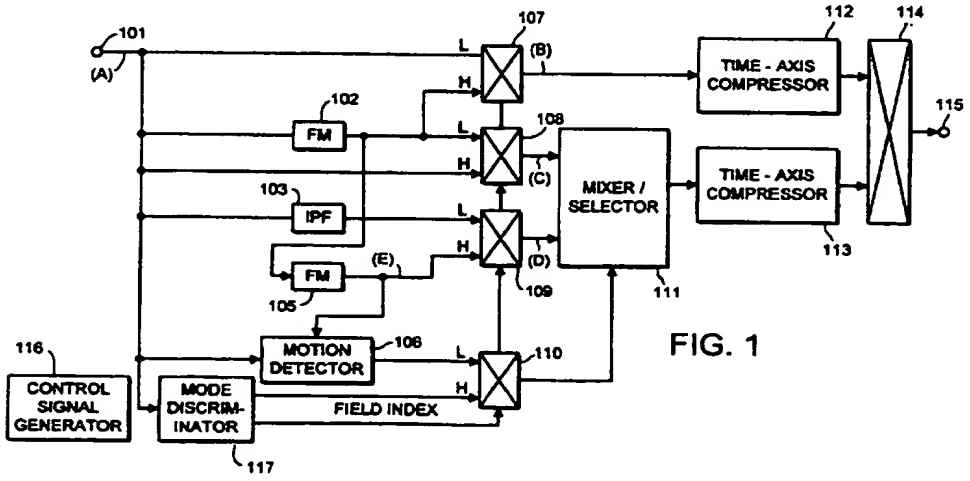

FIG. 1

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

This print takes account of replacement documents submitted after the date of filing to enable the application to comply with the formal requirements of the Patents Rules 1995

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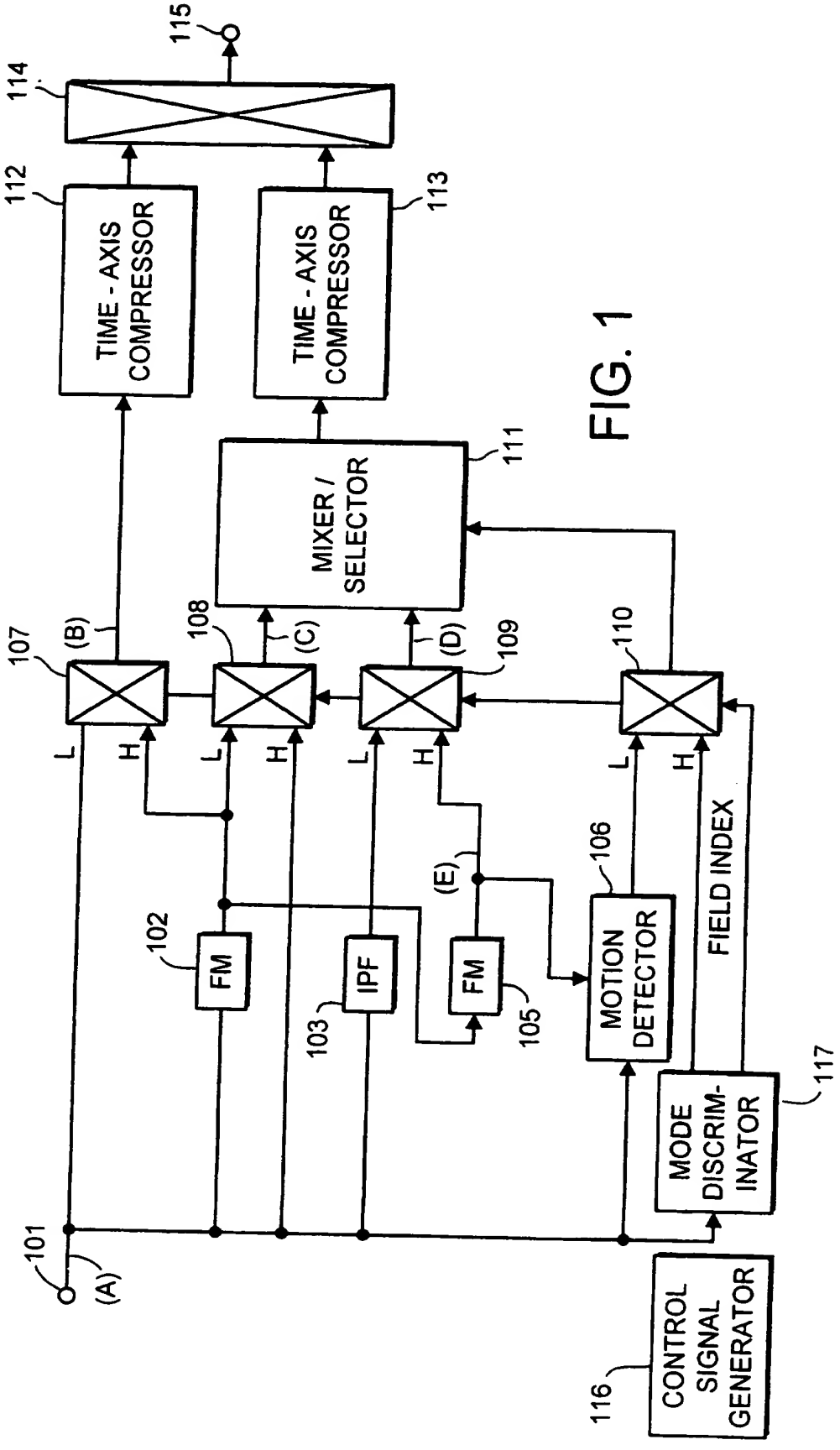
115
114
112
TIME - AXIS COMPRESSOR
113
TIME - AXIS COMPRESSOR
111
MIXER / SELECTOR
107
(B)
108
(C)
(D)
109
110
L
H
L
H
L
H
L
H
(E)
106
102
FM
103
IPF
FM
105
MOTION DETECTOR
FIELD INDEX
MODE DISCRIM-INATOR
117
101
(A)
116
CONTROL SIGNAL GENERATOR

FIG. 1

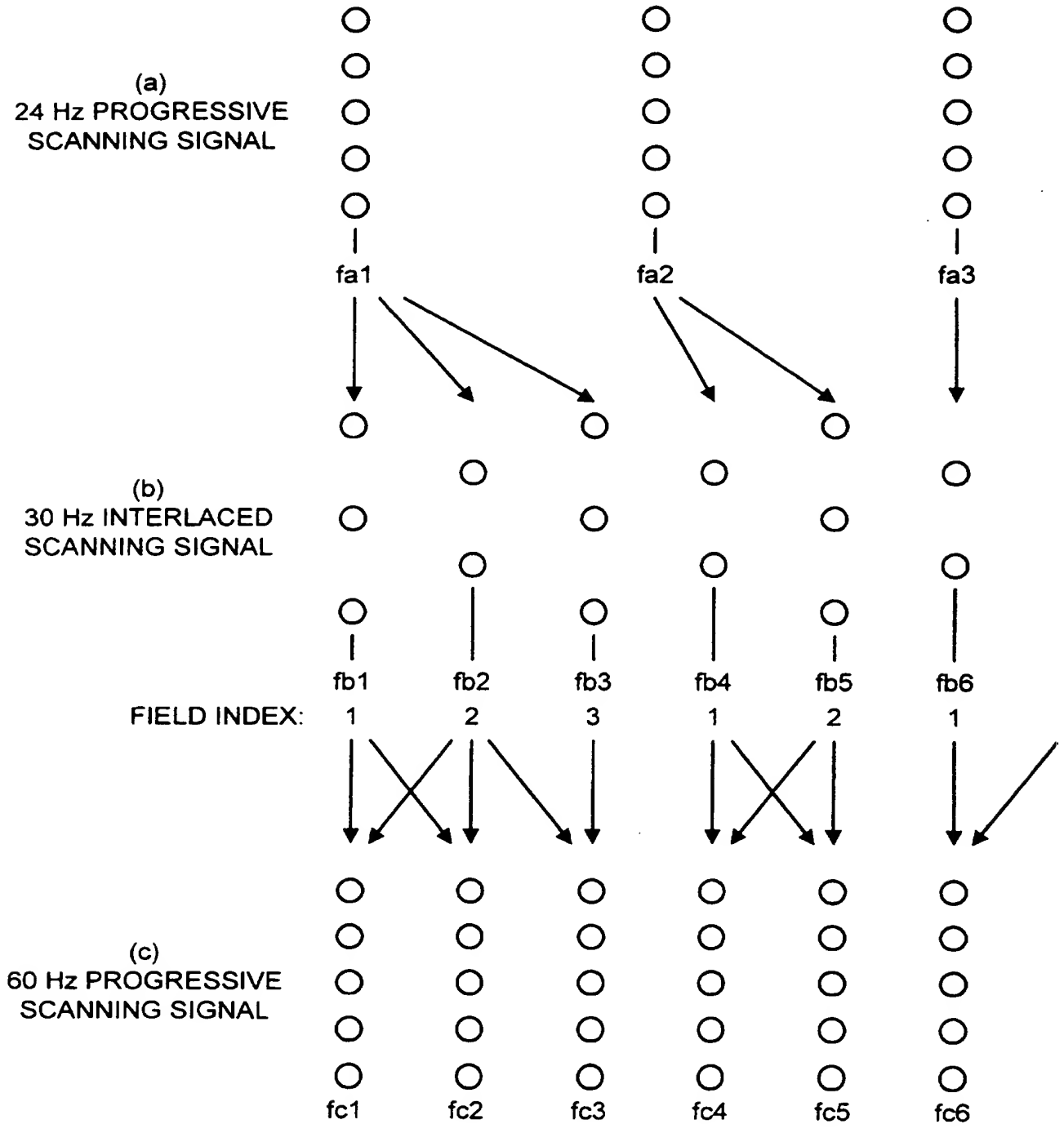
(a)
24 Hz PROGRESSIVE
SCANNING SIGNAL
fa1
fa2
fa3
(b)
30 Hz INTERLACED
SCANNING SIGNAL
fb1
fb2
fb3
fb4
fb5
fb6
FIELD INDEX:
1
2
3
1
2
1
(c)
60 Hz PROGRESSIVE
SCANNING SIGNAL
fc1
fc2
fc3
fc4
fc5
fc6

FIG. 2

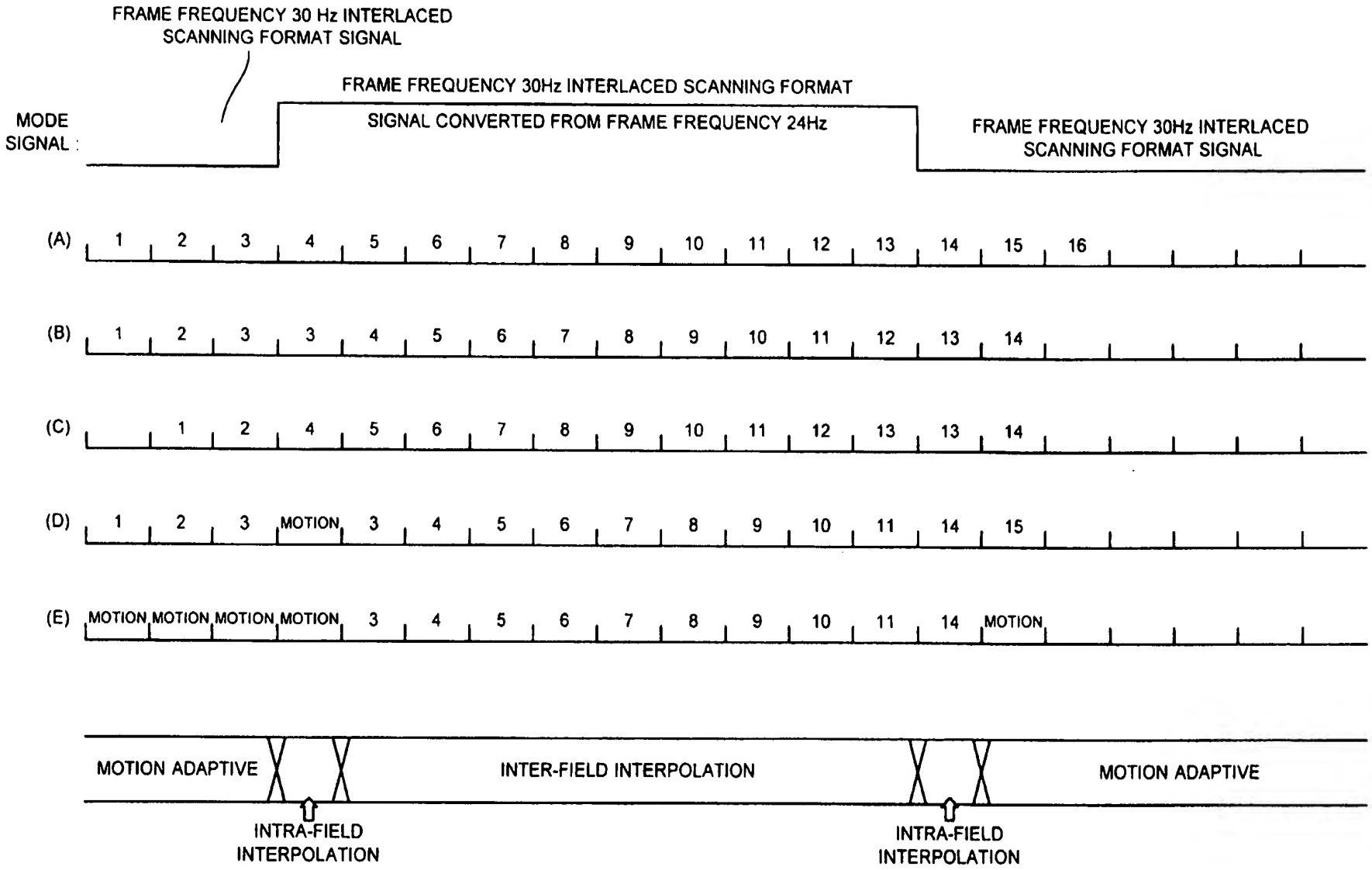
FRAME FREQUENCY 30 Hz INTERLACED SCANNING FORMAT SIGNAL
FRAME FREQUENCY 30Hz INTERLACED SCANNING FORMAT SIGNAL CONVERTED FROM FRAME FREQUENCY 24Hz
FRAME FREQUENCY 30Hz INTERLACED SCANNING FORMAT SIGNAL
MODE SIGNAL
(A) 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
(B) 1 2 3 3 4 5 6 7 8 9 10 11 12 13 14
(C) 1 2 4 5 6 7 8 9 10 11 12 13 13 14
(D) 1 2 3 MOTION 3 4 5 6 7 8 9 10 11 14 15
(E) MOTION MOTION MOTION MOTION 3 4 5 6 7 8 9 10 11 14 MOTION
MOTION ADAPTIVE
INTER-FIELD INTERPOLATION
MOTION ADAPTIVE
INTRA-FIELD INTERPOLATION
INTRA-FIELD INTERPOLATION

FIG. 3

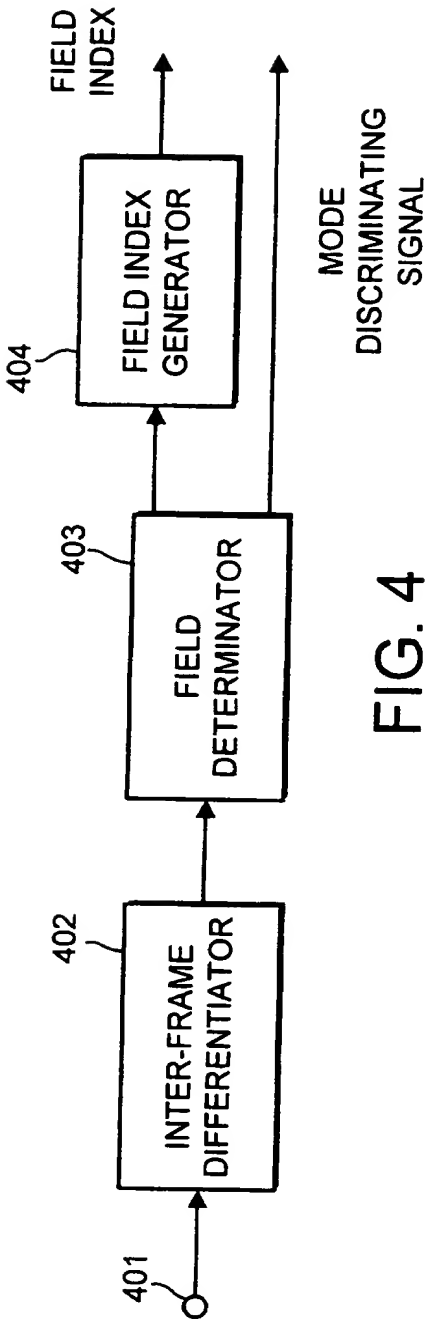
401
402
INTER-FRAME DIFFERENTIATOR
403
FIELD DETERMINATOR
404
FIELD INDEX GENERATOR
FIELD INDEX
MODE DISCRIMINATING SIGNAL

FIG. 4

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VIDEO SIGNAL PROCESSOR

The present invention relates to a video signal processor which generates a progressive scanning format signal from a first input signal which is an interlaced scanning format signal or a second input signal which is an interlaced signal converted from a progressive scanning format signal.

It is well known that film pictures such as movies, etc. are signals having a 24 Hz frame frequency, while the NTSC system, which is widely adopted in e.g., Japan and the U.S.A., employs interlaced scanning format signals with the 30 Hz frame frequency.

In general, broadcast stations convert the film pictures from a progressive scanning signal format with the 24 Hz frame frequency to an interlaced scanning signal format with the 30 Hz frame frequency by processing so-called a 3:2 pull-down conversion before broadcasting the film pictures.

At the receiving side, received signals are displayed by processing in similar ways as the conventional NTSC system TV signals or by processing a frame frequency conversion as disclosed in the Japanese Patent Application; Tokkai-Hei 7-95441.

In recent years, large-sized screen projection TV sets using LCD are put in the market and the display by the progressive scanning is generally used on these display units. Further, as a result of appearance of large-sized screens, more high quality reproduced images are demanded.

When, for instance, an NTSC TV signal (interlaced scanning format

signal with 30 Hz frame frequency) are input, it becomes possible to make the more high quality display by generating and displaying progressive scanning format signals using the progressive scanning conversion method as disclosed in the Japanese Patent Application; Tokkai-Hei 4-157886.

On the other hand, in a DVD system which has recently come onto the market, film pictures such of movies, etc. are recorded on DVD discs at the 24 Hz frame frequency. While, in DVD players the recorded signal are reproduced as a so-called 3:2 pull-down converted 30 Hz interlaced scanning format signals.

When displaying signals on a display unit using LCD, it is possible to obtain high quality reproduced image using a frame frequency conversion technique such as disclosed in the Japanese Patent Application; Tokkai-Hei 7-95441 as described above.

However, reproduced images are not always images of frame frequency 24Hz signals and are considered that the signals are generally contaminated with NTSC system TV signals etc. Although an image memory is indispensable for the progressive scanning and conversion process of these signals, a ratio of an image memory occupied in the entire cost is high. Therefore, it is desirable to share a memory among plural applications.

In this case, when the input signal has transposed from the frame frequency 24Hz video signals to the NTSC system TV signals (interlaced scanning format signal with 30 HZ frame frequency), that is, when the signal to be stored in a memory has transposed, reproduced images may be disturbed. Therefor, conventionally it is required to mask the output

of the memory for a prescribed period for concealing the disturbance of images.

As described above, in a signal processor which shares a part of the processor, for instance, a memory, etc. in the process to re-convert the signal processed the 3:2 pull-down conversion for the film image signal with the 24 Hz frame frequency such as movies to a progressive scanning format signal with the 60Hz frame frequency through its reverse process and for the process to reproduce frame frequency 30Hz interlaced scanning format signals such as NTSC system TV signals by progressively converting, reproduced video signals may be disturbed when the input signal has transposed. It is unfavorable to provide a memory separately to remove this disturbance from the viewpoint of cost.

It is, therefore, an object of the present invention to provide a video signal processor capable of preventing the generation of disturbance of images when the input signal has transposed without requiring increase of a memory.

In order to achieve the above object, in a video signal processor wherein first signal which is interlaced scanning format signal or second signal which was converted from progressive scanning format signal is input, the video signal processor has signal discriminating means for discriminating whether an input signal is the first signal or the second signal, first means for generating an intra-field interpolation signal from the input signal, second means for generating an inter-field interpolation signal from the input signal. third means for delaying the output from the second means by one field, motion detecting means for

detecting the motion of an image from the input signal and the third means, and fourth means, wherein in response to the result of discrimination by the signal discriminating means that the input signal is the first signal, the fourth means generates an interpolation signal by adaptively mixing both outputs from the first and the second means in accordance with the motion detecting signal from the motion detecting means, while in response to the result of discrimination of the signal discriminating means that the input signal is the second signal, the fourth means selectively outputs the second signal as a direct output interpolations signal or the output of the third means as a delayed output interpolation signal.

Additional objects and advantages of the present invention will be apparent to persons skilled in the art from a study of the following description and the accompanying drawings, which are hereby incorporated in and constitute a part of this specification.

For a better understandings of the present invention and many of the attendant advantages thereof, reference will now be made by way of example to the accompanying drawings, wherein:

FIG.1 is a block diagram illustrating the construction of an embodiment of the video signal processor of the present invention;

FIG.2 is a diagram illustrating the operating principle of the progressive scanning conversion when a film picture (frame frequency 24Hz) was processed a 3:2 pull-down conversion and signal which was agreed with frame frequency of NTSC signal;

FIG.3 is a timing diagram for explaining the operation illustrated in FIG.1 when interlaced scanning format signal of frame frequency 30Hz

and interlaced scanning format signal of frame frequency 30Hz converted from progressive scanning format signal of frame frequency 24Hz are successively input in time sequence; and

FIG.4 is a block diagram illustrating one example of the construction of the mode discriminator illustrated in FIG.1.

FIG.1 illustrates the construction of an embodiment of the image signal processor of the present invention.

FIG.3 is a diagram illustrating the timing relation among an input signal (A) to an input terminal 101, outputs (B) – (D) from selectors 107 ~ 109, and the output (E) of a field memory (FM) or a delay circuit 105.

The mode discriminating signal shows the mode discriminated from input signals in a mode discriminator 117 and L shows the frame frequency 30Hz interlaced scanning format signal and H shows the frame frequency 30Hz interlaced scanning format signal converted from a frame frequency 24Hz signal.

(A) is the input signal to he input terminal101, (B)is the output of the selector 107, (C) is the output of the selector 108,(D) is the output of the selector 109 and (E) is the output of the delay circuit 105.

First, the operation when, for instance, a regular signal such as the luminance signal of the NTSC system TV signal is input to the input terminal 101 will be described.

The regular signal input to the input terminal 101 input the selector 107, delay circuit (FM) 102, line interpolating filter (IPF) 103, motion detector 106 and mode discriminator 117.

In the delay circuit 102, the delay process (the inter-field interpolation process) by one field is performed for the input signal

which is then output to the selector 108 and the delay circuit (FM) 105.

In the line interpolating filter 103, the line interpolation signal (the intra-field interpolation signal) is generated and output to the selector 109.

In the motion detector 106, using the signal (A) obtained from the input terminal 101 and the signal (E) obtained from the delay circuit 105, the motions of images are detected and the motion detected signal is output. This motion detected signal is input to the selector 119.

All of the selectors 107~110 are turned to the L terminals when an NTSC system TV broadcast signal has been input.

In other words, the signal which is input through the input terminal 101 is output from the selector 107, the signal which is delayed in the delay circuit 102 is output from the selector 108 and the interpolation signal which is generated through the line interpolating filter 103 is output from the selector 109.

Further, the motion detecting signal which was output from the motion detector 106 is output from a selector 110.

These selector controls are executed by the mode discrimination signal obtained from the input signals in a mode discriminator 117.

In a mixer/selector 111, video signals input via the selectors 108, 109 are adaptively combined based on the motion detecting signal input via the selector 110. That is, when the motion components are determined less, a ratio of the video signal input through the selector 108 is increased. While, when the motion components are determined much, a ratio of the signals input through the selector 109 is increased.

The output of the mixer/selector 111 is input to a time-axis

compressor 113. Further, the output of the selector 107 is input to a time-axis compressor 112. In these circuits 112, 113, signals are output after converted to a speed which is two times of the input signals and input to a selector 114. In the selector 114, the signals input from the time-axis compressors 112, 113 are switched alternately for every horizontal period by the control signal output from the control signal generator 116 and then, output.

The output of the selector 114 is output from the output terminal 115 as the progressive scanning format signal.

When NTSC system TV signals are thus input, the progressive scanning conversion process is carried out according to the motion of images.

Next, the operation when signals of film pictures (24 Hz frame frequency) matched to the frame frequency in the NTSC system signal by prosessing the 3:2 pull-down conversion will be described using FIG.1. In addition, the operating principle of the progressive scanning conversion will be described using FIG. 2.

In FIG. 2, (a), (b) illustrate the state to convert the progressive scanning format signal of frame frequency 24Hz into the interlaced signal of frame frequency 30Hz. Five field interlaced scanning format signal is produced from original 2 frame progressive scanning format signal.

In general, in N frames (N is an integer), three fields of signal are produced from one field signal and in N+1 frames, two field signals are produced from one field signal and the interlaced scanning format signal the 30 Hz frame frequency such as the NTSC system TV signal is

In case of, for instance, on a reproducer such as DVD reproduction device, data are recorded on a recording medium using 24Hz progressive scanning format signal and when reproducing them the data may be output after converting into the NTSC system TV signal. In such a case, it becomes possible to obtain more high quality reproduced image by the progressive scanning conversion by the field superposition rather than the progressive scanning conversion according to the general motion adaptation.

When explaining using FIG. 2, the frame fc1 shown in FIG. 2(c) is generated using the field fb1 and the field fb2 shown in FIG. 2(b).

The frame fc2 shown in FIG.2(c) is generated using the field fb1 and the field fb2 shown in FIG. 2(b) (or using the field fb2 and the field fb3).

The frame fc3 shown in FIG.2(c) is generated using the field fb2 and the field fb3 shown in FIG. 2(b).

The frame fc4 shown in FIG.2(C) is generated using the field fb4 and the field fb5 shown in FIG. (2(b).

The frame fc5 shown in FIG. 2(c) is generated using the field fb4 and he field fb5 shown in FIG. 2(b).

Thus, it becomes possible to obtain higher quality progressive scanned video using signals preceding or succeeding the current field by one field as interpolation signals through the progressive scanning conversion.

Then, the operation of progressive scanning process described above will be explained using FIG.1 and FIG.2.

The signals input to the input terminal 101 are then input to the delay circuit 102, the selector 108 and the mode discriminator 117.

In the mode discriminator 117, the input signal is discriminated and the mode discrimination signal is generated. This mode discrimination signal controls the selectors 107, 108, 109 and 110.

The mode discriminator 117 also generates field indexes of input signal. These field indexes are assigned in order of generation from the original frame signal (FIG. 2(a)), for instance, 1 for the field fb1 in FIG. 2(b), 2 for the filed fb2, 3 for the filed fb3, 1 for the field fb4, 2 for the field fb5.

These field indexes are transmitted to the mixer/selector 111 via the selector 110.

In the delay circuit 102, the input signal is delayed by one field period and transmitted to the selector 107 and at the same time, to the delay circuit 105.

In the delay circuit 105, the input signal is further delayed by one field period and transmitted to the selector 109.

The selectors 108 and 109 are changed over in accordance with the mode discrimination signal from the mode discriminator 117 and input the input signal from the input terminal 101 and the input signal from the delay circuit 105, respectively into the mixer/selector 111.

In the mixer/selector 111, according to the field indexes output from the mode discriminator 117, the outputs of he selectors 108 and 109 are changed over and output. The output of the mixer/selector 111 is time-axis compressed in the time-axis compressor 113 and input to the selector 114.

The output from the selector 107 becomes the output of the delay circuit 102 by the mode discrimination signal from the mode

discriminator 117, input to the time-axis compressor 112 wherein it is time-axis compressed and input to the selector 114.

In the selector 114, the outputs of the time-axis compressors 112 and 113 are alternately changed over every one horizontal period by the control signal which is output from the control signal generator 116 and output. This output of the selector 114 is output from the output terminal 115 as the progressive scanning converted signal.

As described above, only by changing the circuit operation, the progressive scanning and conversion of both originally interlaced scanning format signal of frame frequency 30Hz and interlaced scanning format signal of frame frequency 30Hz converted from progressive scanning format signal of frame frequency 24Hz become possible and further, in a latter case, it is possible to obtain progressive scanned image in more high quality.

Here, when above described two kinds of images are successively input, disturbance may be produced on video depending on signals stored in the delay circuit 105 when images are transposed. Therefore, at a proper time after the input signal has transposed between different types of image signal, it is necessary to differentiate the output of the selector 110 for the progressive scanning conversion from that in the steady state.

When two kinds of operation are executed as described above, different signals are output from the selectors and delay circuits as illustrated in FIG.3.

When, for instance, the interlaced scanning format signal of frame frequency 30Hz is input to he input terminal 101, signals stored for the

motion detection are output (E) from the delay circuit 105 as illustrated in FIG.3.

On the other hand, when the interlaced scanning format signals of frame frequency 30Hz converted from the progressive scanning format signals of frame frequency 24Hz are input to the input terminal 101, the signals input to the input terminal 101 and delayed by two fields are output from the delay circuit 105. These signals may damage images by the progressive scanning conversion at the time when the input signal has transposed.

In this embodiment, the mode discriminator 117 detects the time that the input signal has transposed and controls the output of the line interpolation filter 103 so that it becomes output from the mixer/selector 111 for the period of one field after the input signal has transposed.

Definitely, the mode discriminator 117 outputs L for the period of one field after the input signal has transposed. As a result, the selector 109 selects the output of the line interpolating filter 103 and supplies it to the mixer/selector 111. Further, the selector 110 selects the motion detection signal from the motion detector 106 and supplies to the mixer/selector 111. The motion detection signal in this case becomes a control signal for selecting the output of the selector 109 by the mixer/selector 111.

Thus, the intra-field interpolation is made and it becomes possible to avoid of the damage of images.

FIG.4 illustrates one example of the mode discriminator 117. There are three cases; a case where interlaced scanning format signal of frame frequency 30Hz was generated from progressive scanning format

signal of frame frequency 24Hz and a case to generate three field of interlaced scanning format signal and two fields of interlaced scanning format signal from the progressive scanning one frame.

The field fb1 and the field fb3 illustrated in FIG.4 become the entirely same signals and therefore, if a difference between these two fields is taken, it becomes zero. Shown in FIG.4 is an example of the mode discriminator 117 utilizing this.

The signal input to the input terminal illustrated in FIG.1 is given to the input terminal 401. An inter-field difference of this signal is taken by the inter-frame differentiator 402. This difference is determined in the field determinator 403 as to which fields of the fields fb1 ~ fb5 shown in FIG. 2(b) this difference is equivalent to.

Based on this result of determination, field indexes (1,2,3,1,2,1,2,3,1,...) are output from the field index generator 404.

Further, the field determinator 403 determines whether the input signal is the interlaced scanning format signal of frame frequency 30Hz converted from the progressive scanning format signal of frame frequency 24Hz from the field difference and outputs the mode discrimination signal.

FIG. 4 illustrates one example of a circuit for determining the type of input signal from the signal which is input and it is needless to say that when a signal is applied from the outside, the process will become different.

Further, the construction of assigning field indexes by the mode discriminator 117 when the interlace scanning format signal of frame frequency 30Hz converted from the progressive scanning format signal

of frame frequency 24Hz is input was described above in this embodiment. However, there will be no problem even when the system is so constructed that the field indexes in synchronized with the input signal is separately input and the selectors 107 ~ 110 and the mixer/selector 111 are controlled according to the field indexes.

Further, a case where the interlaced scanning format signal of frame frequency 30Hz converted from the progressive scanning format signal of frame frequency 24Hz was input was described above in this embodiment. However, even when, the signal converted to frame frequency 50Hz, for instance, the PAL signal is input, the same process is applicable at the time that images are changed over. Further, the delay amount of the delay circuits 102,105 are one field, respectively in this case.

Further, the frame frequency of the progressive scanning format film picture signal to be converted into the interlaced scanning format signal is not limited to the 24Hz.

Further, the period that the output of the line interpolating filter 103 is selected by the mixer/selector 111 is not limited to one field period, but it can take two field periods or more.

Further, it is also possible to construct the delay circuits 102 and 105 by a single-chip memory.

As described above, according to the present invention, even when interlaced scanning format signal converted from progressive scanning format signal of frame frequency 24Hz and originally interlaced scanning format signal are successively input, no damage is produced by the image change-over and furthermore, it becomes possible to reproduce

progressive scanning format signal of more higher image quality than before and no memory increase is required.

As described above, the present invention can provide an extremely preferable video signal processor.

While there have been illustrated and described what are at present considered to be preferred embodiments of the present invention, it will be understood by those skilled in the art that various changes and modifications may be made, and equivalents may be substituted for elements thereof without departing from the true scope of the present invention. In addition, many modifications may be made to adapt a particular situation or material to the teaching of the present invention without departing from the central scope thereof. Therefor, it is intended that the present invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out the present invention, but that the present invention includes all embodiments falling within the scope of the appended claims.

The foregoing description and the drawings are regarded by the applicant as including a variety of individually inventive concepts, some of which may lie partially or wholly outside the scope of some or all of the following claims. The fact that the applicant has chosen at the time of filing of the present application to restrict the claimed scope of protection in accordance with the following claims is not to be taken as a disclaimer or alternative inventive concepts that are included in the contents of the application and could be defined by claims differing in scope from the following claims, which different claims may be adopted subsequently during prosecution, for example, for the purposes of a divisional

application.

CLAIMES:

1. In a video signal processor wherein first signal which is interlaced scanning format signal or second signal which was converted from progressive scanning format signal is input, the video signal processor comprising:

signal discriminating means for discriminating whether an input signal is the first signal or the second signal;

first means for generating an intra-field interpolation signal from the input signal;

second means for generating an inter-field interpolation signal from the input signal;

third means for delaying the output from the second means by one field;

motion detecting means for detecting the motion of an image from the input signal and the third means; and

fourth means, wherein

in response to the result of discrimination by the signal discriminating means that the input signal is the first signal, the fourth means generates an interpolation signal by adaptively mixing both outputs from the first and the second means in accordance with the motion detecting signal from the motion detecting means; while

in response to the result of discrimination of the signal discriminating means that the input signal is the second signal, the fourth means selectively outputs the second signal as a direct output interpolations signal or the output of the third means as a delayed

output interpolation signal.

2. A video signal processor as claimed in claim 1, characterized in that it is further provided with:

a memory with a capacity capable of storing at least two fields of the input signal; and

wherein the capacity of the memory by one field is used for the operation of the second means, while the capacity for the other one field is used for the operation of the third means.

3. A video signal processor as claimed in claim 1, wherein it is characterized by that when the input signal transposes from the first signal to the second signal, the fourth means outputs the output of the first means as the interpolation signal output for at least one field after the input signal has transposed.

4. A video signal processor as claimed in claim 1, wherein it is characterized by that when the input signal transposes from the second signal to the first signal, the fourth means outputs the output of the first means as the interpolation signal output for at least one field after the input signal has transposed.

5. A video signal processor as claimed in claim 1, wherein it is characterized by that it is further provided with:

fifth means for inputting an identifying signal in synchronized with the input second signal, and wherein

fourth means selectively outputs the second signal or the output of the third means in response to the identifying signal from the fifth means.

6. A video signal processor as claimed in claim 1, wherein it is characterized by that the signal discriminating means generates identifying signal from the input second signal, and that the fourth means selectively outputs the second signal or the output of the third means in response to the identifying signal.

The Patent Office

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Application No: GB 9811276.6 **Examiner:** John Coules
Claims searched: 1-6 **Date of search:** 7 October 1998

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): H4F FGG,FER,FCD,FGXX

Int Cl (Ed.6): H04N 7/01,5/44,5/46,9/64

Other: Online: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
	None	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.